

BEST AVAILABLE COPY

Appl. No. 10/604,354

Amdt. dated March 16, 2006

Reply to Office action of October 19, 2005

Amendments to the Specification:

Please replace the original paragraph [0021] with the following amended paragraph:

- 5 [0021] Please refer to Fig.5A and Fig.5B. Fig.5A and Fig.5B are cross-sectional views of a CMOS structure of an ESD protection circuit according to the present invention. Similarly, in a [[COMOS]] CMOS process a deep N well 52 is also utilized to isolate a P well 54 and a P-substrate 50. As shown in Fig.5A, the deep N well 52 is first embedded in the P-substrate 50, then the P well 54 is embedded in the deep N well 52. Lastly, an N+
- 10 node 56 is embedded in the P well 54. An NPN BJT uses the N+ node 56 as an emitter, the P well as a base, and the deep N well as a collector, as shown in Fig.5A. An NMOS transistor uses two N+ nodes 56 as a drain and a source, and an insulation layer 58 formed on the channel between the two N+ nodes 56 as a gate, as shown in Fig.5B. The deep N well 52 isolates the NMOS transistor in the P well 54, represented by a circle in the
- 15 NMOS transistor 12 shown in Fig.3.